UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/706,501 | 11/02/2000 | Oleg Rashkovskiy | ITL.0778US (P10142) | 8091 |

21906 7590 12/26/2007

TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

| EXAMINER | |
|---|---|
| SHERKAT, AREZOO | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2131 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 12/26/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov



**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 09/706,501
Filing Date: November 02, 2000
Appellant(s): RASHKOVSKIY ET AL.

Timothy N. Trop
Reg. No. 28,994
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 11/9/2007 appealing from the Office action mailed 4/11/2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**GROUNDS OF REJECTION NOT ON REVIEW**

The following grounds of rejection have not been withdrawn by the examiner, but they are not under review on appeal because they have not been presented for review in the appellant's brief.

Claims are 1-8, 21-28, 79, and 91 rejected under 35 U.S.C. 102(b) as being anticipated by Candelore et al. (U.S. Patent No. 6,061,449).

Claims 10-20, 80-81, and 92-96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Candelore et al., (U.S. Patent No. 6,061,449), in view of Etzel et al., (U.S. Patent No. 6,577,734).

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 6,061,449 | CANDELORE | 5-2000 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Candelore et al., (U.S. Patent No. 6,061,449).

The anticipation rejection of claim 1 is not under review but is presented here as claim 1 is the independent claim on which dependent claim 9 refers to:

Candelore discloses an apparatus comprising:

a storage device to store an original content item in multiple blocks, each block containing at least a single byte (col. 1, lines 50-67 and col. 2, lines 1-7), the blocks stored in a logically linear fashion within the storage allocated for the content item (col. 19, lines 44-67 and col. 20, lines 1-5), a key generator (i.e., address generator) to generate a key according to [an identifier value of another apparatus](col. 24, lines 66-67 and col. 25, lines 1-20)(col. 26, lines 45-60 – wherein unit-dependent keys are used to prevent a pirate from using the key or keys obtained from one unit to either encrypt, encrypt and authenticate, or authenticate program information for another unit), a reorderer for reordering the blocks of an original content item according to [a symmetrical key K](i.e., a block-wise scrambling of N blocks according to an address data signal)(col. 26, lines 14-30), wherein the re-ordered blocks are stored in a non-linear fashion within the storage allocated for the re-ordered content item (col. 23, lines 63-67 and col. 24, lines 1-5).

Regarding claim 9, Candelore discloses wherein the reordered blocks include a first reordered block of a first block size and a second reordered block of a second block size which is different than the first block size (i.e., wherein, as explicitly mentioned in the lines of the cited column, any field can be the basis for re-ordering and bytes, blocks, and chains are arbitrary units for bits ... and the re-ordering operation could allow bytes to be re-ordered across two or more block, blocks across two or more

chains, and chains across two or more program information sequences)(col. 22, lines 25-33).

**(10) Response to Argument**

Appellant argues that "even if Candelore taught using any block size, he does not teach using different block sized within the same re-ordered set" (Remarks, page 10).

Examiner responds that Candelore discloses any field can be the basis for re-ordering and bytes, blocks, and chains are arbitrary units for bits. The fields being re-ordered could be nibbles. Also bytes do not have to be eight bits, nor blocks eight bytes, etc. **The re-ordering operation could allow bytes to be re-ordered across two or more block, blocks across two or more chains, and chains across two or more program information sequences** (col. 22, lines 25-33).

Candelore further discloses when re-ordering occurs across two or more chains, wherein each chain can have the same or different lengths, then two or more chain's worth of block buffers are needed (col. 22, lines 40-47 and col.30, lines 50-64), and different chain lengths may be used for communicating different types of program information from the storage device. Program information requiring less latency can have smaller chain lengths and program information that can tolerate more latency can have longer chain length, thereby saving on the storage of the corresponding authentication information. Thus, the length of each chain can be set according to the processing latency of the program information of the respective chains (col. 27, lines 49-57).

In column 20, lines 29-32, Candelore further teaches that chains lengths can vary between 16 and 32 blocks and are varied on a chain by chain basis according to key and address parameters. The block chaining as offered by Candelore reduces the authentication information overhead while maintaining a desired security level by appending a seven byte block to a chain of 16 to 32 eight byte blocks (col. 21, lines 60-67).

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Arezoo Sherkat/
Arezoo Sherkat
Patent Examiner, GAU 2131

GILBERTO BARRON JR
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Conferees:

Gilberto Barron Jr.
SPE 2132

/Matthew Smithers/
Matthew Smithers
Primary Examiner, GAU 2137